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APPEAL BRIEF FEE TRANSMITTAL

Attorney Docket No.	300.1158
Application Number	10/827,318
Filing Date	April 20, 2004
First Named Inventor	Yoji ASAHI, et al.
Group Art Unit	2893
Examiner Name	TRINH, Hoa B.

AMOUNT ENCLOSED	540.00

FEE CALCULATION (fees effective 10/02/08)

CLAIMS AS AMENDED	Claims Remaining After Amendment	Highest Number Previously Paid For	Number Extra	Rate	Calculations
TOTAL CLAIMS	16	- 20 =	0	X $ 52.00 =	$ 0.00
INDEPENDENT CLAIMS	7	- 7 =	0	X $ 220.00 =	0.00

Since a Notice of Appeal was filed on December 17, 2008, petition is hereby made for an extension to cover the date this reply is filed for which the requisite fee is enclosed (1 month ($130)); (2 months ($490)); (3 months ($1,110)); (4 months ($1,730)); (5 months ($2,350):	
Appeal Brief is enclosed, add ($540.00)	540.00
If Statutory Disclaimer under Rule 20(d) is enclosed, add fee ($140.00)	
Information Disclosure Statement (Rule 1.17(p)) ($180.00)	
Total of above Calculations =	$ 0.00
Reduction by 50% for filing by small entity (37 CFR 1.9, 1.27 & 1.28)	
TOTAL FEES DUE =	$ 540.00

(1) If entry (1) is less than entry (2), entry (3) is "0".

(2) If entry (2) is less than 20, change entry (2) to "20".

(4) If entry (4) is less than entry (5), entry (6) is "0".

(5) If entry (5) is less than 3, change entry (5) to "3".

METHOD OF PAYMENT

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GENERAL AUTHORIZATION

☒ If the above-noted "AMOUNT ENCLOSED" is not correct, the Commissioner is hereby authorized to credit any overpayment or charge any additional fees necessary to:

Deposit Account No.	19-3935
Deposit Account Name	STAAS & HALSEY LLP

☒ The Commissioner is also authorized to credit any overpayments or charge any additional fees required under 37 CFR 1.16 (filing fees) or 37 CFR 1.17 (processing fees) during the prosecution of this application, including any related application(s) claiming benefit hereof pursuant to 35 USC § 120 (e.g., continuations/divisionals/CIPs under 37 CFR 1.53(b) and/or continuations/divisionals/CPAs under 37 CFR 1.53(d)) to maintain pendency hereof or of any such related application.

SUBMITTED BY: STAAS & HALSEY LLP

Typed Name	Paul W. Bobowiec	Reg. No.	47,431
Signature	Paul W. Bobowiec	Date	February 17, 2009

Docket No.: 300.1158

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Yoji ASAHI et al.

Serial No. 10/827,318 Group Art Unit: 2893

Confirmation No. 4043

Filed: April 20, 2004 Examiner: TRINH, Hoa B.

For: SEMICONDUCTOR DEVICE SUBSTRATE

APPELLANTS' APPEAL BRIEF UNDER 37 C.F.R. §41.37

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PO Box 1450
Alexandria, VA 22313-1450

In a Notice of Appeal filed December 17, 2008, the Appellants appealed from the Examiner's Final Office Action mailed September 17, 2008 finally rejecting claims 1-16. Submitted herewith is an Appellants' Appeal Brief under 37 CFR 41.37, and the requisite fees set forth in 37 C.F.R. §41.20(b)(2).

If any further fees are required in connection with this filing, please charge our Deposit Account No. 19-3935.

I. REAL PARTY IN INTEREST

The real party in interest is Shinko Electric Industries, Co., LTD, Nagano, Japan, the assignee of the present above-identified pending US patent application.

II. RELATED APPEALS AND INTERFERENCES

Appellants, Appellants' legal representative, and the assignee do not know of any prior or pending appeals, interferences or judicial proceedings, which may be related to, directly affect or be directly affected by, or have a bearing on, the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 1-16 are rejected. Claims 1, 5, and 11 are objected to.

Claims 1-16 are being appealed.

IV. STATUS OF AMENDMENTS

The Appellants filed an Amendment on December 17, 2008 under 37 C.F.R. § 1.116. As of February 17, 2009, the USPTO PAIR system indicates that the Amendment has not been acted upon by the Examiner. In a telephone conversation on February 17, 2009 between the Examiner and the Appellants' representative, the Examiner indicated that the Amendment should be entered and the entry should be within the next two weeks.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The claims 1-16 are appealed herein. The appealed independent claims are 1, 5, 9, 11, 13, 14, and 16.

Independent claim 1 recites a semiconductor device substrate (for example, semiconductor device substrate of Figs. 1-3) comprised of a core substrate (e.g., core substrate 10 of Figs. 1-3) having, on both main surfaces of which, respective interconnect patterns (e.g., first layer interconnect patterns 12, second layer interconnect patterns 14, and third layer interconnect patterns 16 of Fig. 1) extending through resin layers (e.g., resin layers 18, 20, and 22 of Fig. 1).

The semiconductor device substrate of claim 1 also includes a core substrate (e.g., core substrate 10 of Figs. 1-3) being of a material having a heat expansion coefficient of 4.0 to 10.6 ppm/°C (see, for example, paragraph [0020]), the heat expansion coefficient closer to that of a semiconductor chip (see, for example, paragraph [0020]) than the respective heat expansion coefficients of the resin layers (e.g., resin layers 18, 20, and 22 of Fig. 1) and the interconnect patterns (e.g., first layer interconnect patterns 12, second layer interconnect patterns 14, and third layer interconnect patterns 16 of Fig. 1).

The semiconductor device substrate of claim 1 also includes a resin layer, forming an outermost layer (e.g., solder-resist layers 24 of Fig. 1) of the semiconductor device substrate on each of the main surfaces thereof, of a material having at least one of a higher strength and a higher elongation than a resin material used for inner resin layers of the semiconductor device substrate (see, for example, paragraph [0013]) and preventing cracking and deformation, of the semiconductor device substrate due to thermal stress occurring (see, for example, paragraph [0027]) between two or more of the core substrate (e.g., core substrate 10 of Figs. 1-3), the inner resin layers, and the interconnect patterns (e.g., first layer interconnect patterns 12, second layer interconnect patterns 14, and third layer interconnect patterns 16 of Fig. 1) in the semiconductor device substrate.

The semiconductor device substrate of claim 1 also includes an outermost interconnect pattern (e.g., third layer interconnect patterns 16 of Fig. 1) of the semiconductor device substrate is coated by a resin layer forming an outermost layer of the semiconductor device substrate, and the outermost interconnect pattern (e.g., third layer interconnect patterns 16 of Fig. 1) having a land exposed through the outermost layer formed of the resin layer (see, for example, paragraphs [0020] -[0023]).

Independent claim 5 recites a semiconductor device substrate (for example,

semiconductor device substrate of Figs. 1-3) including a core substrate (for example, core substrate 10 of Figs. 1-3) having, on both main surfaces of which, respective interconnect patterns (e.g., first layer interconnect patterns 12, second layer interconnect patterns 14, and third layer interconnect patterns 16 of Fig. 1) extending through resin layers,

The semiconductor device substrate of claim 5 also includes a core substrate (e.g., core substrate 10 of Figs. 1-3) being of a material having a heat expansion coefficient of 4.0 to 10.6 ppm/°C (see, for example, paragraph [0020]), the heat expansion coefficient closer to that of a semiconductor chip than respective heat expansion coefficients of resin layers and interconnect patterns (e.g., first layer interconnect patterns 12, second layer interconnect patterns 14, and third layer interconnect patterns 16 of Fig. 1) inside the semiconductor device substrate;

The semiconductor device substrate of claim 5 also includes a resin layer, of a material having at least one of a higher strength and a higher elongation (e.g., solder-resist layers 24 of Fig. 1) than a resin material used for the resin layers inside the semiconductor device substrate, forming an outermost layer on each of the opposite main surfaces of the semiconductor device substrate, and

The semiconductor device substrate of claim 5 also includes a resin layer an outermost interconnect pattern (e.g., third layer interconnect patterns 16 of Fig. 1) of the semiconductor device substrate is coated by a resin layer forming an outermost layer of the semiconductor device substrate, and the outermost interconnect pattern (e.g., third layer interconnect patterns 16 of Fig. 1) having a land exposed through the outermost layer formed of the resin layer (see, for example, paragraphs [0020] -[0023]).

Independent claim 9 recites a substrate for a chip (for example, substrate of Figs. 1-3), including a first resin layer forming an outermost layer (e.g., solder-resist layer 24 of Fig. 1) on each of opposite main surfaces of the substrate coating an outermost interconnect pattern (e.g., third layer interconnect patterns 16 of Fig. 1) of the substrate, the outermost interconnect pattern (e.g., third layer interconnect patterns 16 of Fig. 1) having a land exposed through the outermost layer formed of the first resin layer (see, for example, paragraphs [0020] -[0023]).

The substrate for a chip of claim 9 also includes a second resin layer (e.g., resin layer 20 of Fig. 1) underlying the first resin layer (e.g., solder-resist layer 24 of Fig. 1); and a third resin layer (e.g., resin layer 18 of Fig. 1); underlying the second resin layer (e.g., resin layer 20 of Fig. 1); and a core being of a material having a heat expansion coefficient of 4.0 to 10.6 ppm/°C (see, for example, paragraph [0020]), and underlying the third resin layer (e.g., resin layer 18 of

Fig. 1) having, on both main surfaces, respective interconnect patterns (e.g., first layer interconnect patterns 12, second layer interconnect patterns 14, and third layer interconnect patterns 16 of Fig. 1) between the core and at least one of the first resin layer, the second resin layer (e.g., resin layer 20 of Fig. 1), and the third resin layer (e.g., resin layer 18 of Fig. 1), wherein at least one of the first resin layer and the second resin layer (e.g., resin layer 20 of Fig. 1) being of a material having at least one of a higher strength and a higher elongation than a material used for the third resin layer (see, for example, paragraph [0013]).

Independent claim 11 recites a semiconductor device substrate (for example, semiconductor device substrate of Figs. 1-3) comprised of a core substrate (for example, core substrate 10 of Figs. 1-3) having, on both main surfaces of which, respective interconnect patterns (e.g., first layer interconnect patterns 12, second layer interconnect patterns 14, and third layer interconnect patterns 16 of Fig. 1) extending through resin layers, wherein: the core substrate (e.g., core substrate 10 of Figs. 1-3) being of a metal alloy having a heat expansion coefficient of 4.0 to 10.6 ppm/^{o}C (see, for example, paragraph [0020]), the heat expansion coefficient closer to that of a semiconductor chip than the respective heat expansion coefficients of the resin layers and the interconnect patterns(e.g., first layer interconnect patterns 12, second layer interconnect patterns 14, and third layer interconnect patterns 16 of Fig. 1).

The semiconductor device substrate of claim 11 also includes a resin layer, forming an outermost layer (e.g., solder-resist layers 24 of Fig. 1) of the semiconductor device substrate on each of the main surfaces thereof, of a material having at least one of a higher strength and a higher elongation than a resin material used for inner resin layers of the semiconductor device substrate (see, for example, paragraph [0013]) and preventing cracking and deformation, of the semiconductor device substrate due to thermal stress (see, for example, paragraph [0027]) occurring between two or more of the core substrate (e.g., core substrate 10 of Figs. 1-3), the inner resin layers, and the interconnect patterns (e.g., first layer interconnect patterns 12, second layer interconnect patterns 14, and third layer interconnect patterns 16 of Fig. 1) in the semiconductor device substrate, and an outermost interconnect pattern (e.g., third layer interconnect patterns 16 of Fig. 1) of the semiconductor device substrate is coated by a resin layer forming an outermost layer of the semiconductor device substrate (e.g., solder-resist layers 24 of Fig. 1), and the outermost interconnect pattern (e.g., third layer interconnect patterns 16 of Fig. 1) has a land exposed through the outermost layer formed of the resin layer (see, for example, paragraphs [0020] -[0023]).

Independent claim 13 recites a substrate for a chip (for example, substrate of Figs. 1-3), including a first resin layer forming an outermost layer (e.g., solder-resist layers 24 of Fig. 1) on

each of opposite main surfaces of the substrate coating an outermost interconnect pattern of the substrate (e.g., third layer interconnect patterns 16 of Fig. 1), the outermost interconnect pattern (e.g., third layer interconnect patterns 16 of Fig. 1) having a land exposed through the outermost layer formed of the first resin layer (see, for example, paragraphs [0020] -[0023]), a second resin layer (e.g., resin layer 20 of Fig. 1) underlying the first resin layer, a third resin layer underlying the second resin layer, and a metal alloy core having a heat expansion coefficient of 4.0 to 10.6 ppm/°C (see, for example, paragraph [0020]), and underlying the third resin layer having, on both main surfaces, respective interconnect patterns (e.g., first layer interconnect patterns 12, second layer interconnect patterns 14, and third layer interconnect patterns 16 of Fig. 1) between the core and at least one of the first resin layer, the second resin layer (e.g., resin layer 20 of Fig. 1), and the third resin layer, wherein at least one of the first resin layer and the second resin layer (e.g., resin layer 20 of Fig. 1) being of a material having at least one of a higher strength and a higher elongation than a material used for the third resin layer (see, for example, paragraph [0013]).

Independent claim 14 recites a topology for a chip (for example, topology of Figs. 1-3), including a first insulating layer forming an outermost layer on each of opposite main surfaces of a substrate (e.g., solder-resist layers 24 of Fig. 1) coating an outermost interconnect pattern (e.g., third layer interconnect patterns 16 of Fig. 1) of the substrate, the outermost interconnect pattern having a land exposed through the outermost layer formed of the first resin layer (see, for example, paragraphs [0020] -[0023]).

The topology for a chip of claim 14 also includes a second insulating layer (e.g., resin layer 20 of Fig. 1) underlying the first insulating layer; a third insulating layer (e.g., resin layer 18 of Fig. 1), underlying the second insulating layer (e.g., resin layer 20 of Fig. 1); and a metal alloy core (see, for example, paragraph [0025]) having a heat expansion coefficient of 4.0 to 10.6 ppm/ °C (see, for example, paragraph [0020]), and underlying the third insulating layer (e.g., resin layer 18 of Fig. 1), having, on both main surfaces, respective interconnect patterns between the metal alloy core and at least one of the first insulating layer, the second insulating layer, and the third insulating layer (e.g., resin layer 18 of Fig. 1),, wherein at least one of the first insulating layer (e.g., solder-resist layers 24 of Fig. 1) and the second insulating layer (e.g., resin layer 20 of Fig. 1) being of a material having at least one of a higher strength and a higher elongation than a material used for the third insulating layer (e.g., resin layer 20 of Fig. 1 and paragraph [0013]).

Independent claim 16 recites a semiconductor device substrate (for example, semiconductor device substrate of Figs. 1-3) including a core substrate (for example, core

substrate 10 of Figs. 1-3) having a heat expansion coefficient of 4.0 to 10.6 ppm/°C (see, for example, paragraph [0020]).

The semiconductor device substrate of claim 16 also includes an outermost interconnect pattern (e.g., third layer interconnect patterns 16 of Fig. 1) of the semiconductor device substrate coated by a resin layer forming an outermost layer (e.g., solder-resist layer 24 of Fig. 1) of the semiconductor device substrate, and the outermost interconnect pattern (e.g., third layer interconnect patterns 16 of Fig. 1) having a land exposed through the outermost layer formed of the resin layer (see, for example, paragraphs [0020] -[0023]).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The first ground of rejection to be reviewed is whether claims 1-10 and 16 are properly rejected under 35 U.S.C. §103(a) as being unpatentable over Abe (U.S. Pub. 2003/0136577) ("Abe").

The second ground of rejection to be reviewed is whether claims 11-15 are properly rejected under 35 U.S.C. §103(a) as being unpatentable over Abe in view of Nair (U.S. Pub. 2004/0095734) ("Nair").

Claims are each independently patentable over the reference as set forth below, and do not stand or fall together.

VII. ARGUMENT

All arguments are directed to the grounds of rejection. All citations to the "Office Action" refer to the last Office Action of September 17, 2008.

A. FIRST GROUND OF REJECTION

In the Office Action, the Examiner rejects claims 1-10 and 16 under 35 U.S.C. §103(a) as being unpatentable over Abe.

An issue is whether Abe suggests to one skilled in the art to achieve, all of the recited features of claims 1-10 and 16.

A first sub-issue is whether the Examiner has established a *prima facie* case of obviousness based upon Abe.

A second sub-issue is whether the Examiner has provided evidence which as a whole show that the legal determination sought to be proved (i.e., whether the reference teachings establish a *prima facie* case of obviousness) is more probable than not by the preponderance of evidence burden-of-proof standard (37 CFR 1.56(b)).

1. The Law Regarding the Obviousness Issues

To establish obviousness under §103, the Examiner must consider the claimed invention "as a whole," and the prior art must teach or suggest all of the claim features. *See* Manual Of Patent Examining Procedure § 2143.03 (8th ed. Rev. 2 May 2004)("MPEP"); *In re Royka*, 180 U.S.P.Q. 580, 583 (C.C.P.A. 1974); *In re Fine*, 5 U.S.P.Q. 2d 1596, 1599 (Fed. Cir. 1988); *Ruiz v. A.B. Chance Co.*, 69 U.S.P.Q.2d 1686, 1690 (Fed. Cir. 2004). "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). If an independent claim is nonobvious under 35 U.S.C. §103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ 2d 1596 (Fed. Cir. 1988). See Manual Of Patent Examining Procedure § 2143.03 (8th ed. Rev. 5 August 2006)("MPEP").

In *KSR International Co. v. Teleflex* Inc., 82 USPQ2d 1385, 127 SCt 1727, 167 LEd2d 705 (U.S. 2007), the U.S. Supreme Court held that in determining obviousness, one "must ask whether the improvement is more than the predictable use of prior art elements according to their established functions" slip op. 13, 82 USPQ2d at 1396. Furthermore, it is necessary "to determine whether there was an apparent reason to combine the known elements in the fashion claimed" slip op. 14, 82 USPQ2d at 1396.

The Supreme Court further affirmed *In re Kahn,* 441 F. 3d 977, 988 (CA Fed. 2006),

stating: "[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." In this regard, it is respectfully submitted that a single use/mention of a system/method by a single reference is insufficient evidence in the record that it would have been obvious to try the same in the primary reference. As relied upon in the *KSR* decision, any underlying obvious to try rationale still requires evidence in the record of the same.

Impermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art. See MPEP § 2142 Legal Concept of *Prima Facie* Obviousness. Hindsight cannot be used in determining the issue of obviousness and the reviewer must view the prior art without reading into that art the teachings of the application or patent (see Kalman v. Kimberly Clark Corp.713 F.2d 760,218 U.S.P.Q. 781(Fed. Cir. 1983)).

In this regard Appellant submits to the remainder of the decision particularly indicating that regardless of the rejection rationale, the obviousness reason presented by the Examiner must be more than a mere conclusion, i.e., a brief statement that one skilled in the art would "try" the claimed feature is insufficient. Supported "evidence" for the same is same is still required.

An assessment of basic knowledge and common sense that is not based on any evidence in the record lacks substantial evidence support. Id. at 1385, 59 USPQ 2d at 1697. See also *In re Lee*, 277 F.3d 1338, 1344-45, 61 USPQ 2d 1430, 1434-35 (Fed. Cir. 2002). (In reversing the Board's decision, the court stated "'common knowledge and common sense' on which the Board relied in rejecting Lee's application are not the specialized knowledge and expertise contemplated by the Administrative Procedure Act. Conclusory statements such as those here provided do not fulfill the agency's obligation...The board cannot rely on conclusory statements when dealing with particular combinations of prior art and specific claims, but must set forth the rationale on which it relies."). See MPEP § 2144.03.

2. Errors in Examiner's Assertions - Recited Features Not Taught by Art Relied on By Examiner And *Prima Facie* Obviousness Not Established

a) Claim 1 recites a semiconductor device substrate comprised of a core substrate having, on both main surfaces of which, respective interconnect patterns extending through resin layers, wherein: "the core substrate being of a material having a heat expansion coefficient of 4.0 to 10.6 ppm/^{0}C, the heat expansion coefficient closer to that of a semiconductor chip than the respective heat expansion coefficients of the resin layers and the interconnect patterns, and a resin layer, forming an outermost layer of the semiconductor device substrate on each of the main surfaces thereof, of a material having at least one of a higher strength and a higher

elongation than a resin material used for inner resin layers of the semiconductor device substrate and preventing cracking and deformation, of the semiconductor device substrate due to thermal stress occurring between two or more of the core substrate, the inner resin layers, and the interconnect patterns in the semiconductor device substrate, an outermost interconnect pattern of the semiconductor device substrate is coated by a resin layer forming an outermost layer of the semiconductor device substrate, and the outermost interconnect pattern having a land exposed through the outermost layer formed of the resin layer," (emphasis added).

The Action concedes that Abe does not teach:

> [M]aterial for the core substrate is selected so that it is closer to that of a semiconductor chip than the respective heat expansion coefficients of the (third) main resin layers . . .and the interconnect patterns . . . core substrate 10 having respective interconnects patterns . . . extends through the resin layers.

(See, for example, Action at page 4, lines 9 - 12).

However, in support of the rejection the Examiner asserts it would have been obvious:

> [T]o an artisan for optimization and experimentation to select the available materials in Table 1 for . . . preventing cracking, deformation, . . .arising in the substrate due to the thermal stress occurring between the core substrate and the inner resin layers in the substrate and interconnect patterns in the substrate . . . resin layers 14, 22, 26, 30 (fig. 1) may be selected among the disclosed group of materials . . .to provide the outermost layer with the higher strength and elongation than the inner layer because the results are predictable. . . when there is motivation . . .and. . . a finite number of identified, predictable solutions. . .reason to pursue the known options . . . embodiments/materials demonstrate that there were a finite number of known techniques/materials for making a circuit board with high rigidity and reliability. ... reason to try these materials, including core substrate material with a heat expansion of 4-10 ppm/°C, with a reasonable expectation of success.

(Emphasis added, See, for example, Action at page 4, lines 9 -12).

Further, the Examiner asserts:

> With respect to appellants' allegation that Abe does not explicitly teach a resin with a high strength and elongation used in the outermost layer. . . examiner notes that there are a finite number of materials listed in Table 1 of Abe for the resin layers . . .within a general skill of a worker to select the known material.

(See, for example, Action at page 7, lines 4-7).

Appellant submits that the Examiner's assertions are in error. By contrast with the recitation of claim 1, for example, Abe merely discloses various materials used in a circuit board, but does not teach nor suggest, for example, a resin having a high strength and elongation used as a outermost resin layer. (See, for example, Table 1).

Further, in contrast with the recitation of claim 1, Abe teaches:

> [C]arbon fibers arranged in the core layer include . . . carbon fiber groups which are arranged in different direction to intersect each other, whereby a thermal expansion coefficient and strength of the core layer can be adjusted for arrangement directions of the first and the second carbon fiber groups by arranged amounts and cross angles of the first and the second carbon fiber groups. The thermal expansion coefficient and strength of the circuit board can be adjusted corresponding to electronic parts to be mounted.

(See, for example, paragraph [0019]).

That is, Abe teaches an adjustment of properties of a core layer by using different arrangements of carbon fibers, and not by using an adjustment of resins.

Further in contrast with the recitation of claim 1, Abe teaches:

> [T]he thermal expansion coefficients of invar, covar, alloys, such as silicon steel, and a clad material, such as CIC, are substantially the same as the thermal expansion coefficient of silicon. However, they have large specific gravities and add weights unsuitably to be used in the circuit boards, which are processed with the large-sized cores included. Their Young's moduli of elasticity are not high, and large core substrate(s) undesirably have bowing and waves, which causes troubles in the build-up process and in mounting semiconductor elements.

(Emphasis added, see, for example, paragraph [0010]).

That is, Abe teaches that a core, as recited by claim 1, for example, including a "substrate being of a material having a heat expansion coefficient closer to that of a semiconductor chip" is unsuitable. Rather, Abe teaches, instead, a core substrate that is a fiber reinforced metal, and different compositions and rearrangements of a core by rearranging carbon fibers, for example.

Further, Abe does not teach that a material's characteristics of strength and/or elongation are different respectively for an outermost resin layer and inner resin layer.

Appellants submit that many of the Examiner's assertions, are an unsupported taking of Official Notice, and as such can not be properly relied on in support of a finding *prima facie* obviousness. As set forth in MPEP §2144.03:

> It would not be appropriate for the examiner to take official notice of facts without citing a prior art reference where the facts asserted to be well known are not capable of instant and unquestionable demonstration as being well-known The examiner must provide specific factual findings predicated on sound technical and scientific reasoning to support his or her conclusion of common knowledge. . . . The applicant should be presented with the explicit basis on which the examiner regards the matter as subject to official notice **>so as to adequately traverse the rejection< in the next reply after the Office action in which the common knowledge statement was made.

As an example, Appellants submit that the Examiner is taking official notice of facts by

asserting that one of ordinary skill in the art may select from a list of materials in a table, e.g., Table 1 disclosed by Abe including only thermal expansion coefficients of fiber materials and metal materials, and select appropriate material(s) for "the advantage of preventing and cracking, deformation . . . arising in the substrate." (Emphasis added).

As another example, Appellants submit the Examiner is taking official notice of facts by asserting that one of ordinary skill in the art may make a selection, from a table that only lists an overall range of thermal expansion coefficients for polyimide resins, as to which thermal expansion coefficients correlate with those resin layers giving an outermost layer having a higher strength and elongation.

Thus, Appellants submit the Examiner is taking official notice of facts in statements that one of ordinary skill in the art may determine strength and elongation of a resin based on a listed thermal expansion coefficient.

Further, Appellants submit that the Examiner's statement in support of the rejection that a list of materials merely giving ranges of thermal coefficients results in "a finite number of known techniques/materials for making a circuit board with high rigidity and reliability," (emphasis added) is not supported.

Appellants submit, rather, that such a relationship of material identification and circuit board manufacture with "high rigidity and reliability" is not "capable of instant and unquestionable demonstration as being well-known."

The Examiner has not supported the rejection with "specific factual findings predicated on sound technical and scientific reasoning" as required.

Appellants have shown error in the Examiner's obviousness rejection and submit that differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would not have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Further, the recited combination yields more than a predictable result.

Appellants submit that the Examiner's analysis does not satisfy an "obvious to try" standard. Thus, Appellants submit one of ordinary skill in the art would not have reasonably expected that it would impart a similar effect.

Summary

Since Abe does not teach nor suggest all the features recited by claim 1, it is submitted that a *prima facie* case of obviousness is not established. Further, the Examiner has not

provided evidence showing that the reference teaching establish a *prima facie* case of obviousness as more probable than not by the preponderance of evidence burden-of-proof standard. Thus, the Examiner's rejection of claim 1 is incorrect, and the rejection of claim 1 should be reversed.

b) Claim 5

The Examiner rejects claim 5 on the same grounds as claim 1. As discussed in Section VII. A. 2. a) regarding errors in the Examiner's rejection of claim 1, Appellant submits that the Examiner makes similar error in the rejection of claim 5.

That is, as discussed in Section VII. A. 2. a), Abe does not teach a core substrate being of a material having a heat expansion coefficient of 4.0 to 10.6 ppm/°C, "the heat expansion coefficient closer to that of a semiconductor chip than respective heat expansion coefficients of resin layers and interconnect patterns inside the semiconductor device substrate, resin layer, of a material having at least one of a higher strength and a higher elongation than a resin material used for the resin layers inside the semiconductor device substrate, forming an outermost layer on each of the opposite main surfaces of the semiconductor device substrate, and an outermost interconnect pattern of the semiconductor device substrate is coated by a resin layer forming an outermost layer of the semiconductor device substrate, and the outermost interconnect pattern having a land exposed through the outermost layer formed of the resin layer."

Rather, Abe teaches that a core, as recited by claim 5 is unsuitable.

Further, Abe does not teach that a material's characteristics of strength and/or elongation are different respectively for an outermost resin layer and other resin layers.

Thus, the rejection is incorrect since features recited by claim 5 are not taught nor suggested by the art relied on by the Examiner. Therefore, it is submitted that claim 5 patentably distinguishes over the prior art and the Examiner's rejection of claim 5 is incorrect.

c) Claim 9

The Examiner rejects claim 9 on the same grounds as claim 1. As discussed in Section VII. A. 2. a) regarding errors in the Examiner's rejection of claim 1, Appellant submits that the Examiner makes similar error in the rejection of claim 9.

That is, as discussed in Section VII. A. 2. a), Abe does not teach "a core being of a material having a heat expansion coefficient of 4.0 to 10.6 ppm/°C, and underlying the third resin layer having, on both main surfaces, respective interconnect patterns between the core and at least one of the first resin layer, the second resin layer, and the third resin layer, wherein at least one of the first resin layer and the second resin layer being of a material having at least

one of a higher strength and a higher elongation than a material used for the third resin layer." Rather, Abe teaches that a core, as recited by claim 5, for example, is unsuitable.

Further, Abe does not teach that a material's characteristics of strength and/or elongation are different respectively for an outer resin layer and than other resin layers.

Thus, the rejection is incorrect since features recited by claim 9 are not taught nor suggested by the art relied on by the Examiner. Therefore, it is submitted that claim patentably distinguishes over the prior art and the Examiner's rejection of claim 9 is incorrect.

d) Claim 16

The Examiner rejects claim 16 on the same grounds as claim 1. As discussed in Section VII. A. 2. a) ii. regarding errors in the Examiner's rejection of claim 1, Appellant submits that the Examiner makes similar error in the rejection of claim 16.

That is as discussed in Section VII. A. 2. a), Abe does not teach "an outermost interconnect pattern of the semiconductor device substrate coated by a resin layer forming an outermost layer of the semiconductor device substrate, and the outermost interconnect pattern having a land exposed through the outermost layer formed of the resin layer."

Rather, Abe teaches that a core, as recited by claim 15, for example, is unsuitable. Further, Abe does not teach that a material's characteristics of strength and/or elongation are different respectively for an outermost resin layer and than other resin layers.

Thus, the rejection is incorrect since features recited by claim 15 are not taught nor suggested by the art relied on by the Examiner. Therefore, it is submitted that claim 15 patentably distinguishes over the prior art and the Examiner's rejection of claim 1 is incorrect.

e) Claims 2, 3, 4

As recited in claim 2, the semiconductor device substrate of claim 1 includes wherein a further resin layer, under the resin layer forming the outermost layer of the semiconductor device substrate, is made of a resin material having at least one of a higher strength and a higher elongation than the resin material of the inner resin layers in the semiconductor device substrate.

As recited in claim 3, the semiconductor device substrate as set forth in claim 1 includes wherein resin material forming the outermost layer has a fracture strength of at least 90 MPa and an elongation of at least 10%. As recited in claim 4, the semiconductor device substrate as set forth in claim 2, wherein resin material forming the outermost layer has a fracture strength of at least 90 MPa and an elongation of at least 10%.

Claims 2, 3, and 4 are patentable over the cited art for reasons similar to those discussed for claim 1. The art relied on by the Examiner does not teach all of the features of claims 2, 3, and 4 and thus, it is submitted that the rejection of claims 2, 3, and 4 should be reversed.

f) Claims 6, 7

As recited in claim 6, the semiconductor device substrate as set forth in claim 5 includes, wherein a further resin layer, under the resin layer forming the outermost layer of the semiconductor device substrate, is made of a resin material having at least one of a higher strength and a higher elongation than the resin material of the inner resin layers in the semiconductor device substrate.

As recited in claim 7, the semiconductor device substrate as set forth in claim 5 includes, wherein resin material forming the outermost layer has a fracture strength of at least 90 MPa and an elongation of at least 10%. As recited in claim 8, the semiconductor device substrate as set forth in claim 6 includes, wherein resin material forming the outermost layer has a fracture strength of at least 90 MPa and an elongation of at least 10%.

Claims 6, 7, and 8 are patentable over the cited art for reasons similar to those discussed above for claim 5 . The art relied on by the Examiner does not teach all of the features of claims 6, 7, and 8 and thus, it is submitted that the rejection of claims 6, 7, and 8 should be reversed.

B. SECOND GROUND OF REJECTION

In the Office Action, the Examiner rejects claims 11-15 under 35 U.S.C. §103(a) as being unpatentable over Abe in view of Nair. (Action at page 6).

An issue is whether a combination of Abe and Nair suggests to one skilled in the art to achieve, the recited features of claims 11-15. A first sub-issue is whether the Examiner has established a *prima facie* case of obviousness based upon Abe and Nair. A second sub-issue is whether the Examiner has provided evidence which as a whole show that the legal determination sought to be proved (i.e., whether the reference teachings establish a *prima facie* case of obviousness) is more probable than not by the preponderance of evidence burden-of-proof standard (37 CFR 1.56(b)).

1. Errors in Examiner's Assertions - Recited Features Not Taught by Art Relied on By Examiner And *Prima Facie* Obviousness Not Established

a) Claim 11

Claim 11 recites a semiconductor device substrate comprised of a core substrate having, on both main surfaces of which, respective interconnect patterns extending through resin layers, wherein: "a core substrate being of a metal alloy having a heat expansion coefficient of 4.0 to

10.6 ppm/°C, the heat expansion coefficient closer to that of a semiconductor chip than the respective heat expansion coefficients of the resin layers and the interconnect patterns, and a resin layer, forming an outermost layer of the semiconductor device substrate on each of the main surfaces thereof, of a material having at least one of a higher strength and a higher elongation than a resin material used for inner resin layers of the semiconductor device substrate and preventing cracking and deformation, of the semiconductor device substrate due to thermal stress occurring between two or more of the core substrate, the inner resin layers, and the interconnect patterns in the semiconductor device substrate, an outermost interconnect pattern of the semiconductor device substrate is coated by the resin layer forming the outermost layer of the semiconductor device substrate, and the outermost interconnect pattern has a land exposed through the outermost layer formed of the resin layer," (emphasis added).

In support of the rejection of claim 11, the Examiner asserts that since Nair teaches:

> [A]n analogous device having a core substrate . . . made of an iron-nickel alloy . . . for providing a high capacitance substrate. . . it would have obvious . . . to [sic-modify] material of the core substrate of Abe with the iron nickel alloy material, as taught by Nair, for providing the advantage.

(See, Action at page 6, lines 11- 15).

Appellants submit that Abe does not teach nor suggest a core substrate being of a metal alloy having a heat expansion coefficient of 4.0 to 10.6 ppm/°C, and Abe does not teach nor suggest an outermost interconnect pattern of the semiconductor device substrate is coated by a resin layer forming an outermost layer of the semiconductor device substrate, and the outermost interconnect pattern has a land exposed through the outermost layer formed of the resin layer.

Appellants submit that the teachings of Nair do not overcome these deficiencies in the teachings of Abe. Appellants further submit the Examiner's assertions are in error. By contrast with the recitations of claim, Abe specifically discloses:

> As shown in Table 1, the thermal expansion coefficients of the metal materials are larger than the thermal expansion coefficient 3.5 ppm/.degree. C. of silicon, but the thermal expansion coefficient of carbon is 0 2 ppm/.degree. C., which is smaller than that of silicon. The thermal expansion coefficient of SiC is substantially equal to that of silicon. . . . found that a composite material of the metal material and the fiber material is formed to thereby form the core substrate of a thermal expansion coefficient which is approximate to that of silicon.

(Emphasis added, See, paragraph [0053]).

That is, since Abe teaches a core substrate needs to be a composite material since metal alloys have thermal coefficients of expansion larger than the thermal expansion coefficient

of silicon, Appellants submit that one of ordinary skill in the art would not have modified Abe and Nair, in a manner as the Examiner suggests.

Further, Appellants submit that the Examiner's proposal to modify Abe with Nair is unreasonable since as set forth in MPEP §2143.01, a claimed combination cannot change the principle of operation of the primary reference or render the reference inoperable for its intended propose and that it is improper to combine references where the references teach away from their combination.

The Examiner also asserts:

> [A]pplicants allege that Abe teaches a metal alloy that has a thermal coefficient expansion larger than silicon. First, appellants' argument is flaw [sic] because appellants fail to particularly point out which material in Table 1 is the metal alloy taught by Abe. Second, the examiner uses Nair for the teaching of a metal alloy as claimed which cures Abe's deficiency.

(Emphasis added, See, for example, Action at page 7, lines 12-14).

Appellants submit that the Examiners comments regarding the Appellants traverse of the rejection of claim 11 in a previous Amendment filed June 13, 2008 ("previous Amendment") are unfounded. In the previous Amendment, Appellants traversed the rejection by also arguing that a proposed combination of Abe and Nair was unreasonable since Abe teaches a core substrate should be a composite material since metal alloys have thermal coefficients of expansion larger than the thermal expansion coefficient of silicon. (See, previous Amendment, page 11, line 35 - page 12, line 2). Appellants submit this argument is not flawed, as the Examiner asserts. Rather, Appellants submit that the Examiner's interpretation of Abe is in error.

Summary

Since the art of record does not teach nor suggest all the features recited by claim 11, it is submitted that a *prima facie* case of obviousness is not established and the rejection of claim 1 should be reversed.

b) Claim 13

The Examiner rejects claim 13 on the same grounds as claim 11. As discussed in Section VII. B. 1. a) regarding errors in the Examiner's rejection of claim 11, Appellant submits that the Examiner makes similar errors in the rejection of claim 13.

That is, as discussed in Section VII. B. 1. a), a combination of Abe and Nair do not teach "at least one of the first resin layer and the second resin layer being of a material having at least one of a higher strength and a higher elongation than a material used for the third resin layer."

Thus, the rejection is incorrect since features recited by claim 13 are not taught nor

suggested by the art relied on by the Examiner. Therefore, it is submitted that claim 13 patentably distinguishes over the prior art and the Examiner's rejection of claim 13 is incorrect.

c) Claim 14

The Examiner rejects claim 14 on the same grounds as claim 11. As discussed in regarding errors in the Examiner's rejection of claim 11, Appellant submits that the Examiner makes similar error in the rejection of claim 14.

That is, as discussed in Section VII. B. 1. a), a combination of Abe and Nair do not teach "wherein at least one of the first insulating layer and the second insulating layer being of a material having at least one of a higher strength and a higher elongation than a material used for the third insulating layer."

Thus, the rejection is incorrect since features recited by claim 14 are not taught nor suggested by the art relied on by the Examiner.

Therefore, it is submitted that claim 14 patentably distinguishes over the prior art and the Examiner's rejection of claim 14 is incorrect.

d) Claim 12

Claim 12 recites the semiconductor device substrate according to claim 11, wherein the metal alloy being an iron-nickel alloy. Claim 12 is patentable over the cited art for reasons similar to those discussed above for claim 11.

Since the art relied on by the Examiner does not teach all of the features of claim 11 and thus, it is submitted that the rejection of claim 12 should be reversed.

e) Claim 15

Claim 15 recites the topology for a chip according to claim 14, wherein the metal alloy core being an iron-nickel alloy. Claim 15 is patentable over the cited art for reasons similar to those discussed above for claim 14 .

Since the art relied on by the Examiner does not teach all of the features of claim 11 and thus, it is submitted that the rejection of claim 14 should be reversed.

CONCLUSION

In view of the foregoing remarks, Appellants submit that pending appealed claims 1-16 patentably distinguish over the relied upon prior art. Reversal of the Examiner's rejections is respectfully requested.

The Commissioner is hereby authorized to charge any additional fees required in connection with the filling of this Appeal Brief to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

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VIII. CLAIMS APPENDIX

1. A semiconductor device substrate comprised of a core substrate having, on both main surfaces of which, respective interconnect patterns extending through resin layers, wherein:

the core substrate being of a material having a heat expansion coefficient of 4.0 to 10.6 ppm/°C, the heat expansion coefficient closer to that of a semiconductor chip than the respective heat expansion coefficients of the resin layers and the interconnect patterns, ~~and~~

a resin layer, forming an outermost layer of the semiconductor device substrate on each of the main surfaces thereof, of a material having at least one of a higher strength and a higher elongation than a resin material used for inner resin layers of the semiconductor device substrate and preventing cracking and deformation, of the semiconductor device substrate due to thermal stress occurring between two or more of the core substrate, the inner resin layers, and the interconnect patterns in the semiconductor device substrate, and

an outermost interconnect pattern of the semiconductor device substrate is coated by a resin layer forming an outermost layer of the semiconductor device substrate, and the outermost interconnect pattern having a land exposed through the outermost layer formed of the resin layer.

2. The semiconductor device substrate as set forth in claim 1, wherein a further resin layer, under the resin layer forming the outermost layer of the semiconductor device substrate, is made of a resin material having at least one of a higher strength and a higher elongation than the resin material of the inner resin layers in the semiconductor device substrate.

3. The semiconductor device substrate as set forth in claim 1, wherein resin material forming the outermost layer has a fracture strength of at least 90 MPa and an elongation of at least 10%.

4. The semiconductor device substrate as set forth in claim 2, wherein resin material forming the outermost layer has a fracture strength of at least 90 MPa and an elongation of at least 10%.

5. A semiconductor device substrate, comprising:

a core substrate having, on both main surfaces of which, respective interconnect patterns extending through resin layers,

the core substrate being of a material having a heat expansion coefficient of 4.0 to 10.6 ppm/°C, the heat expansion coefficient closer to that of a semiconductor chip than respective heat expansion coefficients of resin layers and interconnect patterns inside the semiconductor device substrate;

a resin layer, of a material having at least one of a higher strength and a higher elongation than a resin material used for the resin layers inside the semiconductor device substrate, forming an outermost layer on each of the opposite main surfaces of the semiconductor device substrate, and

an outermost interconnect pattern of the semiconductor device substrate is coated by a resin layer forming an outermost layer of the semiconductor device substrate, and the outermost interconnect pattern having a land exposed through the outermost layer formed of the resin layer.

6. The semiconductor device substrate as set forth in claim 5, wherein a further resin layer, under the resin layer forming the outermost layer of the semiconductor device substrate, is made of a resin material having at least one of a higher strength and a higher elongation than the resin material of the inner resin layers in the semiconductor device substrate.

7. The semiconductor device substrate as set forth in claim 5, wherein resin material forming the outermost layer has a fracture strength of at least 90 MPa and an elongation of at least 10%.

8. The semiconductor device substrate as set forth in claim 6, wherein resin material forming the outermost layer has a fracture strength of at least 90 MPa and an elongation of at least 10%.

9. A substrate for a chip, comprising:

a first resin layer forming an outermost layer on each of opposite main surfaces of the substrate coating an outermost interconnect pattern of the substrate, the outermost interconnect pattern having a land exposed through the outermost layer formed of the first resin layer;

a second resin layer underlying the first resin layer;

a third resin layer underlying the second resin layer; and

a core being of a material having a heat expansion coefficient of 4.0 to 10.6 ppm/°C,

and underlying the third resin layer having, on both main surfaces, respective interconnect patterns between the core and at least one of the first resin layer, the second resin layer, and the third resin layer,

wherein at least one of the first resin layer and the second resin layer being of a material having at least one of a higher strength and a higher elongation than a material used for the third resin layer.

10. The substrate according to claim 9, wherein material forming the first resin layer has a fracture strength of at least 90 MPa and an elongation of at least 10%.

11. A semiconductor device substrate comprised of a core substrate having, on both main surfaces of which, respective interconnect patterns extending through resin layers, wherein:

the core substrate being of a metal alloy having a heat expansion coefficient of 4.0 to 10.6 ppm/°C, the heat expansion coefficient closer to that of a semiconductor chip than the respective heat expansion coefficients of the resin layers and the interconnect patterns, and

a resin layer, forming an outermost layer of the semiconductor device substrate on each of the main surfaces thereof, of a material having at least one of a higher strength and a higher elongation than a resin material used for inner resin layers of the semiconductor device substrate and preventing cracking and deformation, of the semiconductor device substrate due to thermal stress occurring between two or more of the core substrate, the inner resin layers, and the interconnect patterns in the semiconductor device substrate,

an outermost interconnect pattern of the semiconductor device substrate is coated by a resin layer forming an outermost layer of the semiconductor device substrate, and the outermost interconnect pattern has a land exposed through the outermost layer formed of the resin layer.

12. The semiconductor device substrate according to claim 11, wherein the metal alloy being an iron-nickel alloy.

13. A substrate for a chip, comprising:

a first resin layer forming an outermost layer on each of opposite main surfaces of the substrate coating an outermost interconnect pattern of the substrate, the outermost interconnect pattern having a land exposed through the outermost layer formed of the first resin layer;

a second resin layer underlying the first resin layer;

a third resin layer underlying the second resin layer; and

a metal alloy core having a heat expansion coefficient of 4.0 to 10.6 ppm/°C and underlying the third resin layer having, on both main surfaces, respective interconnect patterns between the core and at least one of the first resin layer, the second resin layer, and the third resin layer,

wherein at least one of the first resin layer and the second resin layer being of a material having at least one of a higher strength and a higher elongation than a material used for the third resin layer.

14. A topology for a chip, comprising:

a first insulating layer forming an outermost layer on each of opposite main surfaces of a substrate coating an outermost interconnect pattern of the substrate, the outermost interconnect pattern having a land exposed through the outermost layer formed of the first resin layer;

a second insulating layer underlying the first insulating layer;

a third insulating layer underlying the second insulating layer; and

a metal alloy core having a heat expansion coefficient of 4.0 to 10.6 ppm/ °C, and underlying the third insulating layer having, on both main surfaces, respective interconnect patterns between the metal alloy core and at least one of the first insulating layer, the second insulating layer, and the third insulating layer,

wherein at least one of the first insulating layer and the second insulating layer being of a material having at least one of a higher strength and a higher elongation than a material used for the third insulating layer.

15. The topology for a chip according to claim 14, wherein the metal alloy core being an iron-nickel alloy.

16. A semiconductor device substrate, comprising:

a core substrate having a heat expansion coefficient of 4.0 to 10.6 ppm/°C; and

an outermost interconnect pattern of the semiconductor device substrate coated by a resin layer forming an outermost layer of the semiconductor device substrate, and the outermost interconnect pattern having a land exposed through the outermost layer formed of the resin layer.

IX. EVIDENCE APPENDIX

None

X. RELATED PROCEEDINGS APPENDIX

None